CLAIMS

1. A DRAM memory including an array of storage elements arranged in lines and columns, and for each column:

write means capable of biasing at least a selected one of the elements to a charge level chosen from among a first predetermined high level and a second predetermined low level, combined with read means adapted to determining whether a stored charge level is greater or smaller than a predetermined charge level; and

isolation means adapted to isolating the array from the read and/or write means,

each column further including refreshment means, distinct from the read and write means, for increasing, beyond the first and second predetermined levels, the charge stored in a storage element.

2. The memory of claim 1, wherein said refreshment means are formed of a P-channel dual-gate MOS transistor, interposed between a high supply rail and a node of interconnection of drains of two P-channel dual-gate MOS transistors, sources of which form input/output terminals, each of which is connected to a gate of the other transistor.

3. The memory of claim 1, wherein said isolation means include, interposed between each output of the array and one of the input/output terminals of the read-write means, an N-channel dual-gate MOS transistor.

4. The memory of claim 1, wherein each column also includes a stage for precharging the array.

5. The memory of claim 4, wherein said precharge stage includes, interposed between each output of the network and a precharge supply source, an N-channel dual-gate MOS transistor.

6. The memory of claim 1, wherein each column also includes a stage for precharging and balancing the read means.

7. The memory of claim 6, wherein the precharging and balancing stage includes,

interposed between two read terminals of the read means, three MOS transistors of the same type with a common gate, two first ones of which are series-connected between the read terminals, their common point being connected to a precharge supply source, and the last one directly short-circuitry the read terminals.

8. A method for writing a datum into the memory of claim 1, including the step of biasing the isolation means so that they are partially open, and enabling the refreshment means.

9. A method for writing a datum into the memory of claim 1, including the step of biasing the isolation means so that they are fully open, and enabling the refreshment means.

10. A method for controlling the memory of claim 3, including providing, for the isolating means, a three-level control signal, a first level completely activating the isolation means, a second low level completely inhibiting the isolation means and a third level being adapted to activating or inhibiting each N-channel dual-gate MOS transistor according to the state of the input/output terminal of the read-write means associated therewith.